UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,671	04/23/2001	Katsuaki Matsui	32011-171408	1009

26694 7590 12/23/2002

VENABLE, BAETJER, HOWARD AND CIVILETTI, LLP
P.O. BOX 34385
WASHINGTON, DC 20043-9998

EXAMINER	
WEST, JEFFREY R	
ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 12/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/839,671	Applicant(s) MATSUI, KATSUAKI
	Examiner Jeffrey R. West	Art Unit 2857

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 12-15, and 20* is/are rejected.

7)☒ Claim(s) *8-11 and 16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to because they do not have sufficiently descriptive Labels. Blank boxes in drawings should be labeled descriptively unless it is a well-known component.

Specification

3. The disclosure is objected to because of the following informalities:

On page 5, lines 9-10, "to make the invention understand" should be ---to make the invention understandable---.

On page 8, lines 20 and 25, page 16, line 5, and page 19, lines 21 and 25, Applicant incorrectly labels the output of pads 109 and 510, as "Q" instead of "TQ" as it is illustrated in the corresponding Figures.

On page 19, line 22, "to the multiplexer" should be ---through the multiplexer---.

On page 19, line 22, the specification states "D is output from the pad 511" while Figure 5 shows "MCLK" as being output from pad "511". Similarly, on page 20, line 4, the specification states "pad 511 outputs the test clock TCLK".

On page 20, line 1, the specification states "clock TCLK is input from the pad 508" while Figure 5 shows "TD" as being input from pad 508.

On page 20, line 4, "is measured" should be ---for measurement---.

Appropriate correction is required.

Claim Objections

4. Claim 1 is objected to because of the following informalities:

In claim 1, "guiding a test clock which has been supplied" should be ---guiding a test clock, which has been supplied---.

Appropriate correction is required.

5. Claims 8-11 and 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

7. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 includes the limitation, "wherein said third signal path is formed so that the wiring delay time from said signal output terminal of said circuit block to said dummy latch is substantially the same as the wiring delay time from said signal output terminal of said circuit block to said latch". When written in this form, the claim is equating the timing delay of a path with itself. Since this condition will always be true, it is suggested that Applicant re-word this claim to better point out the instant invention.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,696,771 to Beausang et al. in view of U.S. Patent No. 6,144,262 to Kingsley and further in view of U.S. Patent No. 5,875,114 to Kagatani et al.

Beausang discloses a method and apparatus for performing partial unscan and near full scan tests on a macro cell/circuit block to which an input signal is input at an input clock and which outputs an output signal of a value corresponding to said input signal comprising a first signal path for guiding a test input signal to the signal

input terminal of the macro cell/circuit block, a second signal path for guiding a test clock to the clock input terminal of the macro cell/circuit block, and a third signal path for guiding a test output signal, which has been output from the signal output terminal of the macro cell/circuit block (column 6, lines 50-63, column 10, lines 42-63 and Figures 5A-5D). Beausang discloses including a selecting multiplexer on the first signal path for switching between data from the previous macro cell/circuit block, applied during normal operation, and test data, applied during testing operation (column 12, lines 39-47). Beausang also discloses testing the macro cell/circuit block until preset timing criteria of the signal paths are met (column 4, lines 33-54)

As noted above, Beausang teaches many features of the claimed invention, and although Beausang teaches determining the timing relations of signal paths, Beausang does not teach a method for determining signal wiring delays.

Kingsley teaches a system and method for measuring a signal propagation delay through a series of memory devices (abstract) including applying a test mode/enable signal to the tester that causes the application of a test clock which is routed to an output (i.e. guiding a test clock input to said clock input terminal to an output) to determine the clock-to-out delays of the device (i.e. delay of the third path above) (column 5, line 61 to column 6, line 2) wherein the delay measuring period of the test clock has a timing equal to that of the path delay (column 6, lines 40-43 and Figure 3).

Kagatani teaches an interconnect delay calculation apparatus and path delay value verification apparatus for designing semiconductor circuits and circuit model

data storage devices, more specifically applicable to previous inventions which determine delay times in macro cells (column 1, lines 10-17), wherein the delay calculation includes a method for calculating the delay caused by physical characteristics of the wiring (i.e. wiring delay) (column 4, line 55 to column 5, line 18).

It would have been obvious to one having ordinary skill in the art to modify the invention of Beausang to include the specifics for determining signal path delays, as taught by Kingsley, because Kingsley teaches a method for determining the timing of signal paths of interest, as would be applicable in the invention of Beausang (column 12, lines 34-40), using a method applicable in an integrated circuit that is not directly accessible while eliminating the need for applying guard bands (column 2, lines 11-29)

It would have been obvious to one having ordinary skill in the art to modify the invention of Beausang and Kingsley to include determining the wiring delay in addition to the propagation delay, as taught by Kagatani, because Kagatani teaches that determining path delay without accounting for wiring delay provides incorrect results (column 1, lines 28-36) and suggests that the combination would provide the desired accuracy (column 22, lines 30-39).

Although the invention of Beausang, Kingsley, and Kagatani doesn't specifically disclose routing the signal paths to output pads, the combination does disclose including input/output pads to control physical specifications (Beausang et al., column 19, lines 23-34) as well as measuring output path delay values, and since it

is well known in the art to supply desired output signals to pads of an integrated circuit to allow the operator to perform measurements, this feature is not considered patentable over the prior art.

Further, since Beausang teaches including a selecting multiplexer to switch between a test input and a normal input to provide test and normal output, respectively, and since Kingsley includes using a test clock selected only during testing operation, it would have been obvious to one having ordinary skill in the art to include selecting multiplexers on all of the paths of interest that supply a prescribed normal signal, only during normal operation, and supply the necessary test signals, only during testing operation, because the combination would have insured that user received the desired test data from the circuit during test operation, and that test data would not disrupt the device under normal operation.

10. Claims 12, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang in view of Kingsley and Kagatani, and further in view of U.S. Patent No. 4,878,209 to Bassett et al.

As noted above, Beausang in combination with Kingsley and Kagatani teaches all the features of the claimed invention except for including a dummy latch for receiving the output signal and a path for guiding the latch output to a pad for measurement.

Bassett teaches a macro performance test for determining an on-chip delay time between a test signal and an input signal for enabling the macro, thereby allowing

accurate timing measurements comprising generating an enabling signal for a macro latch, determining an on-chip delay time between the output latch enabling signal and an input signal, for synchronization, supplying the synchronized output latch enabling signal to the output latch for a period of time equal to the access time of the macro, and testing the latched output data from the macro (column 2, lines 51-64).

It would have been obvious to one having ordinary skill in the art to modify the invention of Beausang, Kingsley, and Kagatani to include a dummy latch for receiving the output signal and a path for guiding the latch output to a pad for measurement, as taught by Wells, because, as suggested by Wells, the combination would have provided a method for allowing the user to control the access time of the macro in order to provide accurate timing measurements (column 5, lines 33-47).

Further, although Bassett doesn't specifically disclose introducing the test output signal at the same operating speed of the latch, since it is well known in the art that the clocking speed of the latch determines the output speed of the latch, it is considered inherent that the resulting test output of the latch would operate at the latch clocking speed.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,434,727 to Ishii et al. teaches methods of making a hard macro cell using a timing interval.

U.S. Patent No. 6,272,439 to Buer et al. teaches a programmable delay path circuit and operating point frequency detection apparatus.

U.S. Patent No. 6,189,121 to Ogawa teaches semiconductor device containing a self-test circuit for measuring propagation delay.

U.S. Patent No. 5,821,786 to Nozuyama et al. teaches a semiconductor integrated circuit having a function for evaluating AC performance.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
December 16, 2002

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800